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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/364,786	07/30/1999	Radhika Thekkath	0077.20	9876

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EXAMINER
CHUNG, DANIEL J

ART UNIT	PAPER NUMBER
2672	14

DATE MAILED: 07/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/364,786	THEKKATH ET AL.	
	Examiner	Art Unit	
	Daniel J Chung	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12,13* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-41 are presented for examination. This office action is in response to the RCE filed on 4-14-2003.

Information Disclosure Statement

Receipt is acknowledged of Applicant's Information Disclosure Statement of 4-14-2003, 4-23-2003, which has been placed in the application file and considered by the Examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lapidous et al (6,285,779) in view of Heinrich ("MIPS R4000 Microprocessor User's Manual).

Regarding claim 1, Lapidous et al discloses that the claimed feature of a method for performing computer graphics calculations, method comprising: representing a vertex in a computer graphics image with a plurality of coordinates (See col 1 line 38-col

2 line 6, col 5 line 8-42, col 6 line 53-col 7 line 15, col 17 line 47-50); transforming plurality of coordinates into a plurality of transformed coordinates (See Fig 1A, Fig 1B, col 1 line 38-col 2 line 6, col 5 line 8-42, col 6 line 53-col 7 line 15, col 9 line 50-60, col 17 line 41-46); using a floating point magnitude compare instruction to perform a magnitude comparison between at least a portion of plurality of transformed coordinates and a value representing a plurality of edges of a specified view volume, wherein comparison results for at least three view volume edges are obtained. (See Fig 17, Abstract line 7-13, col 4 line 9-37, col 5 line 8-col 6 line 7, col 18 line 56+)

Lapidous et al does not explicitly disclose that the processing of floating point compare operations. However, such limitation is shown in the teaching of Heinrich. ["the floating-point compare (C.fmt.cond) instructions interpret the contents of two FPU registers (fs, ft) in the specified format (fmt) and arithmetically compare them"] (See p.171, Table 6-12, B-19) The motivation would have been to reduces the number of floating point calculations with view volume, to utilize faster integer calculations (such as addition, subtraction, shifts and masks), to eliminate repetitious calculations, to utilize both hardware and software optimization. Therefore, it would have been obvious to one skilled in the art to incorporate the teaching of Heinrich into the teaching of Lapidous et al. Although Heinrich does not specifically mentioned that two input values (fs, ft) are compared their absolute values using the compare condition specified in the instruction, taking the arithmetic absolute value of (fs,ft), which also suggested by Heinrich (See B-13), are necessarily required for comparing the distances("absolute magnitude") of

Lapidous's teaching, as it is commonly known that the value of magnitude can not be negative values. Therefore, it would have been obvious to one skilled in the art to incorporate the 'the floating-point compare instructions' of Heinrich into the teaching of Lapidous with taking the absolute values of two inputs (fs,ft), thereby correctly providing the output of "absolute magnitude representable in the floating-point format" in Lapidous.

Regarding claim 2, Lapidous et al discloses that plurality of transformed coordinates are processed in parallel. (See col 1 line 38-48, col 9 line 50-60)

Regarding claim 3, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that setting a plurality of condition code bits to one or more specific states to indicate results of magnitude comparison. (See p.159, p.161, p.170)

Regarding claim 4, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that specifying a compare condition in floating point magnitude compare instruction. (See p.159, p.161, p.170)

Regarding claim 5, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that setting one of plurality of condition code bits to indicate true if an

associated compare condition is true and setting one condition code bit to indicate false if associated compare condition is false. (See p.159, p.161, p.170)

Regarding claim 6, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that converting a plurality of fixed point values into a plurality of floating point values using a first convert instruction. (See p.170, B-10)

Regarding claim 7, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that first convert instruction is a CVT.PS.PW instruction. (See B-9, B-10)

Regarding claim 8, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that converting a plurality of floating point values into a plurality of fixed point values using a second convert instruction. (See p.170, B-10, B-21, B-23)

Regarding claim 9, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that second convert instruction is a CVT.PS.PW instruction. (See B-9, B-10)

Regarding claim 10, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that floating point magnitude compare instruction is a CABS instruction. (See p.171, B-9, B-10, B-19)

Regarding claims 11-19, claims 11-19 are similar in scope to the claims 1 and 3-10, and thus the rejections to claims 1 and 3-10 hereinabove are also applicable to claims 11-19.

Regarding claims 20-21 and 24-25, claims 20-21 and 24-25 are similar in scope to the claims of 1-3, and thus the rejections to claims of 1-3 hereinabove are also applicable to claims 20-21 and 24-25.

Regarding claim 22, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that first instruction is part of a general purpose instruction set architecture. (See p.159, p.161, p.170, p.171)

Regarding claim 23, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that first instruction is part of an application specific extension to a general purpose instruction set architecture. (See p.159, p.161, p.170, p.171)

Regarding claim 26, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that first instruction is executed in a single clock cycle. (See p.159, p.161, p.170, p.171)

Regarding claims 27-28, claims 27-28 are similar in scope to the claim 1, and thus the rejection to claim 1 hereinabove is also applicable to claims 27-28.

Regarding claim 29, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that plurality of operands are in a paired-single data format. (See p.159, p.161, p.170, p.171)

Regarding claims 30-37, claims 30-37 are similar in scope to the claims of 2 and 20-23 and thus the rejections to claims of 2 and 20-23 hereinabove are also applicable to claims 30-37.

Regarding claims 38-41, claims 38-41 are similar in scope to the claims of 1,6 and 29 and thus the rejections to claims of 1,6 and 29 hereinabove are also applicable to claims 38-41.

Claims 1-41 are once again rejected under 35 U.S.C. 103(a) as being unpatentable over Lapidous et al (6,285,779) in view of Heinrich ("MIPS R4000 Microprocessor User's Manual) and further in view of Dubey et al (6,298,365).

Regarding claim 1, Lapidous et al discloses that the claimed feature of a method for performing computer graphics calculations, method comprising:

Representing a vertex in a computer graphics image with a plurality of coordinates (See col 1 line 38-col 2 line 6, col 5 line 8-42, col 6 line 53-col 7 line 15, col 17 line 47-50)

Transforming plurality of coordinates into a plurality of transformed coordinates (See Fig 1A, Fig 1B, col 1 line 38-col 2 line 6, col 5 line 8-42, col 6 line 53-col 7 line 15, col 9 line 50-60, col 17 line 41-46)

Using a floating point magnitude compare instruction to perform a magnitude comparison between at least a portion of plurality of transformed coordinates and a value representing a plurality of edges of a specified view volume, wherein comparison results for at least three view volume edges are obtained. (See Fig 17, Abstract line 7-13, col 4 line 9-37, col 5 line 8-col 6 line 7, col 18 line 56+)

Lapidous et al does not explicitly disclose that the processing of floating point compare operations. However, such limitation is shown in the teaching of Heinrich. (See p.171, B-19) The motivation would have been to reduces the number of floating point calculations with view volume, to utilize faster integer calculations (such as addition, subtraction, shifts and masks), to eliminate repetitious calculations, to utilize both hardware and software optimization. Therefore, it would have been obvious to one skilled in the art to incorporate the teaching of Heinrich into the teaching of Lapidous et al.

The combination of Lapidous and Heinrich do not specifically disclose that the floating point magnitude compare instruction takes two input values specified by the instruction and compares their absolute values using the compare condition specified in the instruction. However, such limitation is shown in the teaching of Dubey et al. ["floating-point bounds comparison function"] (See Abstract, col 1 line 41-60, col 3 line 35-col 4 line 24, col 7 line 1+) It would have been obvious to one skilled in the art to incorporate the teaching of Dubey into the teaching of Lapidous, in order to provide "a quick and easy (less complex) comparison function within computer instruction set architectures" (See col 1 line 35-36, col 1 line 52-60 in Dubey), as such improvement is also advantageously desirable in the teaching of Lapidous for providing "the absolute magnitude" representable by the floating-point format with easy manner.

Regarding claim 2, Lapidous et al discloses that plurality of transformed coordinates are processed in parallel. (See col 1 line 38-48, col 9 line 50-60)

Regarding claim 3, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that setting a plurality of condition code bits to one or more specific states to indicate results of magnitude comparison. (See p.159, p.161, p.170)

Regarding claim 4, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that specifying a compare condition in floating point magnitude compare instruction. (See p.159, p.161, p.170)

Regarding claim 5, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that setting one of plurality of condition code bits to indicate true if an associated compare condition is true and setting one condition code bit to indicate false if associated compare condition is false. (See p.159, p.161, p.170)

Regarding claim 6, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that converting a plurality of fixed point values into a plurality of floating point values using a first convert instruction. (See p.170, B-10)

Regarding claim 7, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that first convert instruction is a CVT.PS.PW instruction. (See B-9, B-10)

Regarding claim 8, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that converting a plurality of floating point values into a plurality of fixed point values using a second convert instruction. (See p.170, B-10, B-21, B-23)

Regarding claim 9, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that second convert instruction is a CVT.PS.PW instruction. (See B-9, B-10)

Regarding claim 10, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that floating point magnitude compare instruction is a CABS instruction. (See p.171, B-9, B-10, B-19)

Regarding claims 11-19, claims 11-19 are similar in scope to the claims 1 and 3-10, and thus the rejections to claims 1 and 3-10 hereinabove are also applicable to claims 11-19.

Regarding claims 20-21 and 24-25, claims 20-21 and 24-25 are similar in scope to the claims of 1-3, and thus the rejections to claims of 1-3 hereinabove are also applicable to claims 20-21 and 24-25.

Regarding claim 22, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that first instruction is part of a general purpose instruction set architecture. (See p.159, p.161, p.170, p.171)

Regarding claim 23, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that first instruction is part of an application specific extension to a general purpose instruction set architecture. (See p.159, p.161, p.170, p.171)

Regarding claim 26, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that first instruction is executed in a single clock cycle. (See p.159, p.161, p.170, p.171)

Regarding claims 27-28, claims 27-28 are similar in scope to the claim 1, and thus the rejection to claim 1 hereinabove is also applicable to claims 27-28.

Regarding claim 29, refer to the discussion for the claim 1 hereinabove, Heinrich further discloses that plurality of operands are in a paired-single data format. (See p.159, p.161, p.170, p.171)

Regarding claims 30-37, claims 30-37 are similar in scope to the claims of 2 and 20-23 and thus the rejections to claims of 2 and 20-23 hereinabove are also applicable to claims 30-37.

Regarding claims 38-41, claims 38-41 are similar in scope to the claims of 1,6 and 29 and thus the rejections to claims of 1,6 and 29 hereinabove are also applicable to claims 38-41.

Response to Arguments/Amendments

Applicant's arguments with respect to claims 1-41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Chung whose telephone number is (703) 306-3419. He can normally be reached Monday-Thursday and alternate Fridays from 7:30am- 5:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael, Razavi, can be reached at (703) 305-4713.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

djc
June 27, 2003

JEFFREY BRIER
PRIMARY EXAMINER